11. The structure of claim **7** wherein the width of said second portion is greater than the width of said first portion.

12. The structure of claim **11** wherein the width of the top surface of said first portion is in the range of 30-250 Angstroms.

13. A method for making a semiconductor structure comprising:

forming a substrate;

forming a conductive region, wherein said conductive region is above said substrate;

forming a multi-component dielectric spacer comprised of a first portion and a second portion, wherein the height of said first portion is less than the height of a sidewall of said conductive region, wherein said first portion is above said substrate and directly adjacent to said sidewall of said conductive region, wherein said second portion is directly above said first portion and is directly adjacent to said sidewall of said conductive region, and wherein the dielectric constant of said first portion is lower than the dielectric constant of said second portion.

14. The method of claim **13** wherein the dielectric constant of said second portion is at least twice the dielectric constant of said first portion.

15. The method of claim **13** wherein the dielectric constant of said first portion is in the range of 2.0-4.0, and wherein the dielectric constant of said second portion is in the range of 4.0-7.5.

16. The method of claim **15** wherein said first portion is comprised of a material selected from the group consisting of silicon dioxide, a porous film and a fluorinated oxide, and wherein said second portion is comprised of a material selected from the group consisting of silicon nitride, silicon oxy-nitride and carbon-doped silicon nitride.

17. The method of claim **13** wherein the width of said second portion is greater than the width of said first portion.

18. The method of claim **17** wherein the width of the top surface of said first portion is in the range of 30-250 Angstroms.

19. A method for making a semiconductor device comprising:

forming a substrate;

forming a gate dielectric layer, wherein said gate dielectric layer is above said substrate;

forming a gate electrode, wherein said gate electrode is above said gate dielectric layer;

forming a first gate isolation spacer, wherein said first gate isolation spacer is directly adjacent to a sidewall of said gate electrode;

removing a portion of said substrate to form an etched-out region;

forming a source/drain region above said etched-out region, wherein the top surface of said source/drain region is above the top surface of said substrate, and wherein a sidewall of said source/drain region is directly adjacent to said first gate isolation spacer;

removing said first gate isolation spacer to provide a trench between said sidewall of said source/drain region and said sidewall of said gate electrode;

forming a first dielectric material layer above said source/drain region, directly adjacent to said sidewall of said gate electrode, above said gate electrode and in said trench;

removing the portion of said first dielectric material layer that is not in said trench to provide a first portion of a second gate isolation spacer, wherein said first portion of said second gate isolation spacer is above said substrate and directly in between said sidewall of said gate electrode and said sidewall of said source/drain region;

forming a second dielectric material layer above said source/drain region, directly adjacent to said sidewall of said gate electrode, above said gate electrode and directly above said first portion of said second gate isolation spacer; and

etching said second dielectric material layer to provide a second portion of said second gate isolation spacer, wherein said second portion of said second gate isolation spacer is directly above said first portion of said second gate isolation spacer and is directly adjacent to said sidewall of said gate electrode.

20. The method of claim **19** wherein the dielectric constant of said second portion of said second gate isolation spacer is at least twice the dielectric constant of said first portion of said second gate isolation spacer.

21. The method of claim **19** wherein the dielectric constant of said first portion of said second gate isolation spacer is in the range of 2.0-4.0, and wherein the dielectric constant of said second portion of said second gate isolation spacer is in the range of 4.0-7.5.

22. The method of claim **21** wherein said first portion of said second gate isolation spacer is comprised of a material selected from the group consisting of silicon dioxide, a porous film and a fluorinated oxide, and wherein said second portion of said second gate isolation spacer is comprised of a material selected from the group consisting of silicon nitride, silicon oxy-nitride and carbon-doped silicon nitride.

23. The method of claim **19** wherein the width of said second portion of said second gate isolation spacer is greater than the width of said first portion of said second gate isolation spacer.

24. The method of claim **23** wherein the width of the top surface of said first portion of said second gate isolation spacer is in the range of 30-250 Angstroms.

25. The method of claim **19** wherein said first gate isolation spacer is comprised of a low-temperature furnace oxide.

26. The method of claim **19** wherein said sidewall of said source/drain region is facet-less.

27. The method of claim **26** wherein said trench has a height in the range of 50-1000 Angstroms.

28. The method of claim **19** wherein said sidewall of said source/drain region is faceted.

29. The method of claim **19** wherein the top surface of said first portion of said second gate isolation spacer is flush with the top surface of said source/drain region.

30. The method of claim **19** wherein said first portion of said second gate isolation spacer has a faster etch rate than said second portion of said second gate isolation spacer.

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